Class / Semester / Subject Code: F.Y.B.Sc.(C.S.) / I /-USCS101 –Computer organization and design

Date : 18.11.2019   Time : (2½ Hours)   Total Marks: 75

N.B.   (1)   All questions are compulsory.
       (2)   Figures to the right indicate marks for respective sub questions.
       (3)   Figures to the right indicate marks.
       (4)   Illustrations, in-depth answers and diagram will be appreciated.
       (5)   Mixing of sub-question is not allowed.

Q.1)   Attempt all. (Each of 5 marks)   (15)
     (a)   Multiple Choice Questions (Choose the correct alternative.)   (5)
     (i)   _____ bus structure is usually used to connect I/O devices.
            (a)   Rambus   (b)   Single bus
            (c)   Star bus   (d)   Multiple bus
     (ii)   ___ is used to store data in registers.
            (a)   D Flip-flop   (b)   JK Flip-flop
            (c)   RS Flip-flop   (d)   None of these
     (iii) When we subtract -3 from 2 , the answer in 2's complement form is __.
            (a)   1001   (b)   1101
            (c)   0101   (d)   0001
     (iv)   If one of the input to an OR gate is high then its output will be _____
            (a)   Medium   (b)   Low
            (c)   High   (d)   No output
     (v)   One Byte is equivalent to _____ bits.
            (a)   2   (b)   8
            (c)   16   (d)   6

     (b)   Fill in the blanks. (DATA, register, 2^n, 2^n+1, TEXT, low, interrupt)   (5)
     (i)   The fastest data access is provided using ____.
     (ii)   If one of the inputs to an AND gate is low its output will be _____.
     (iii) _____ is a type of exceptions.
     (iv)   A K-map of n variables contains _____ cells.
     (v)   Execution section in MIPS begins with ____ label.

     (c)   Short Answers Write answers in one or two lines.   (5)
     (i)   Define RTN.
     (ii)   Define cache.
     (iii) What is BUS?
     (iv)   Define Combinational circuit.
     (v)   State the role of ALU.

Q.2)   Attempt the following:(ANY THREE) (Each of 5 marks)   (15)
     (i)   Reduce the given circuit using k-mapping technique. Given set
            Σ m(2,4,5,6,10)
     (ii)   Explain with a diagram the design of ripple carry adder.
     (iii) Explain with neat diagram conceptual view of the hardware needed for
            computation.
     (iv)   Explain the concept of universal gate.
     (v)   List and explain in brief main features of fourth generation computers.

(vi) Convert the following: (each step carries marks)
    a) $(110110)_2 = (\_\_)_{10}$ b) $(10001110)_2 = (\_\_)_{10}$
    c) $(52)_8 = (\_\_\_)_{10}$ d) $(2FA)_{16} = ( )_{10}$

Q.3)   Attempt the following:(ANY THREE) (Each of 5 marks)   (15)
(i)   What is ISA? List and explain types of ISA available.
(ii)   List the steps of machine instruction needed to execute Swapping of two numbers.
(iii)   Define the following terms: instruction stack, subroutines and Memory Operations.
(iv)   Explain with example sequence of actions needed to fetch and execute an unconditional branch instruction
(v)   What is Memory organization? Define memory hierarchy with a neat diagram.
(vi)   Explain Big - Endian and Little - Endian Assignments.

Q.4)   Attempt the following:(ANY THREE) (Each of 5 marks)   (15)
(i)   List and explain with neat diagram main components of processor.
(ii)   Write a program in MIPS to display multiples of 2 from 1 to 10.
(iii)   Explain with example sequence of actions needed to fetch and execute an unconditional branch instruction
(iv)   What is Basic I/O system? Define its importance in Computer organization.
(v)   Explain the following terms used in processor management:
    a) Interrupts   b) Exceptions   c) Instruction pipeline
(vi)   What is Data Transfer? Explain using different modes of I/O Data Transfer.

Q.5)   Attempt the following:(ANY THREE) (Each of 5 marks)   (15)
(i)   What are the differences between the main memory and secondary memory?
(ii)   Find the minimum cost SOP implementation of :
    $f(a,b,c,d) = \Sigma\ m(3,7,11,12,13,14,15)$
(iii)   What are addressing modes? Why different addressing modes are required? Explain different RISC - type addressing modes.
(iv)   Define the following terms: Assembly directives, word size and Memory Operations
(v)   Using RISC instructions demonstrate use of loop statement. Explain using any example
(vi)   Explain the following terms used in processor management:
    a) interfaces   b) Peripheral Devices   c) Instruction pipeline
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